IN THE SPECIFICATION

Please amend the specification as follows:

Replace the paragraph on page 16, between lines 21-28 of the specification with the following:

A shorting transistor is connected across the terminals of the second capacitor C_2 and controlled by $\frac{1}{1}$ $\frac{1}{1}$ $\frac{1}{1}$ $\frac{1}{1}$ $\frac{1}{1}$ $\frac{1}{1}$ As in the previous circuits, this enables a gate-source voltage to be stored on the capacitor C_1 bypassing capacitor C_2 . A charging transistor associated with control line A_4 is connected between a power supply line 50 and the drain of the drive transistor T_D . This provides a charging path for the capacitor C_1 , together with a discharging transistor associated with control $\frac{1}{1}$ $\frac{1}{1}$ $\frac{1}{1}$ $\frac{1}{1}$ $\frac{1}{1}$ and connected between the gate and drain of the drive transistor.

Replace the paragraph spanning pages 16-17, between page 16, line 29, and page 17, line 4 of the specification with the following:

The circuit operates by holding A_2 —and A_3 — A_2 —and A_3 —high, A_4

is then held high momentarily to pull the cathode high and charge the capacitor C_1 to a high gate-source voltage. The power line is at ground to reverse bias the LED. T_D then discharges to its threshold voltage (the discharge transistor associated with line A_1 being turned on) and it is stored on C_1 . A_2 and A_3 A_2 and A_3 are then brought low, A_1 is brought high and the data is addressed onto C_2 . The power line is then brought high again to light the LED.